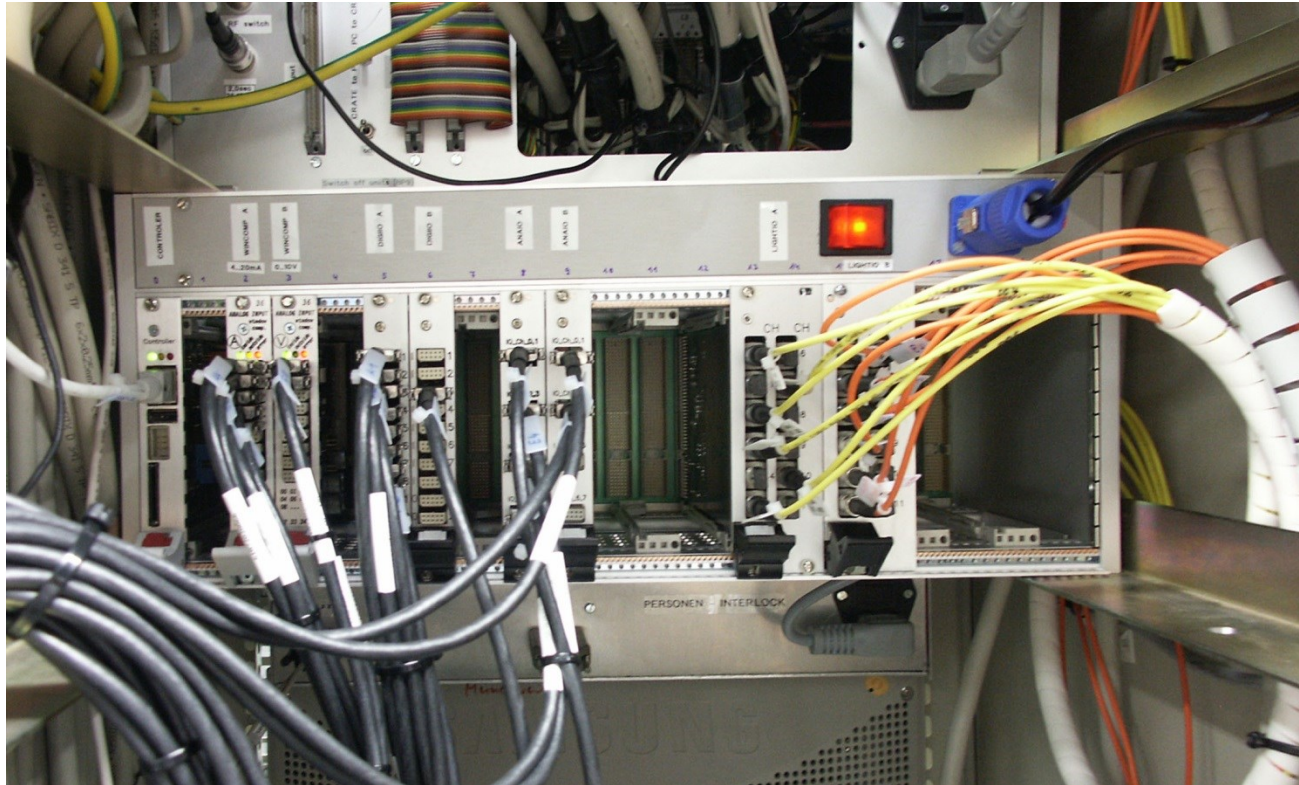# RF Interlock Overview

Marek Penno
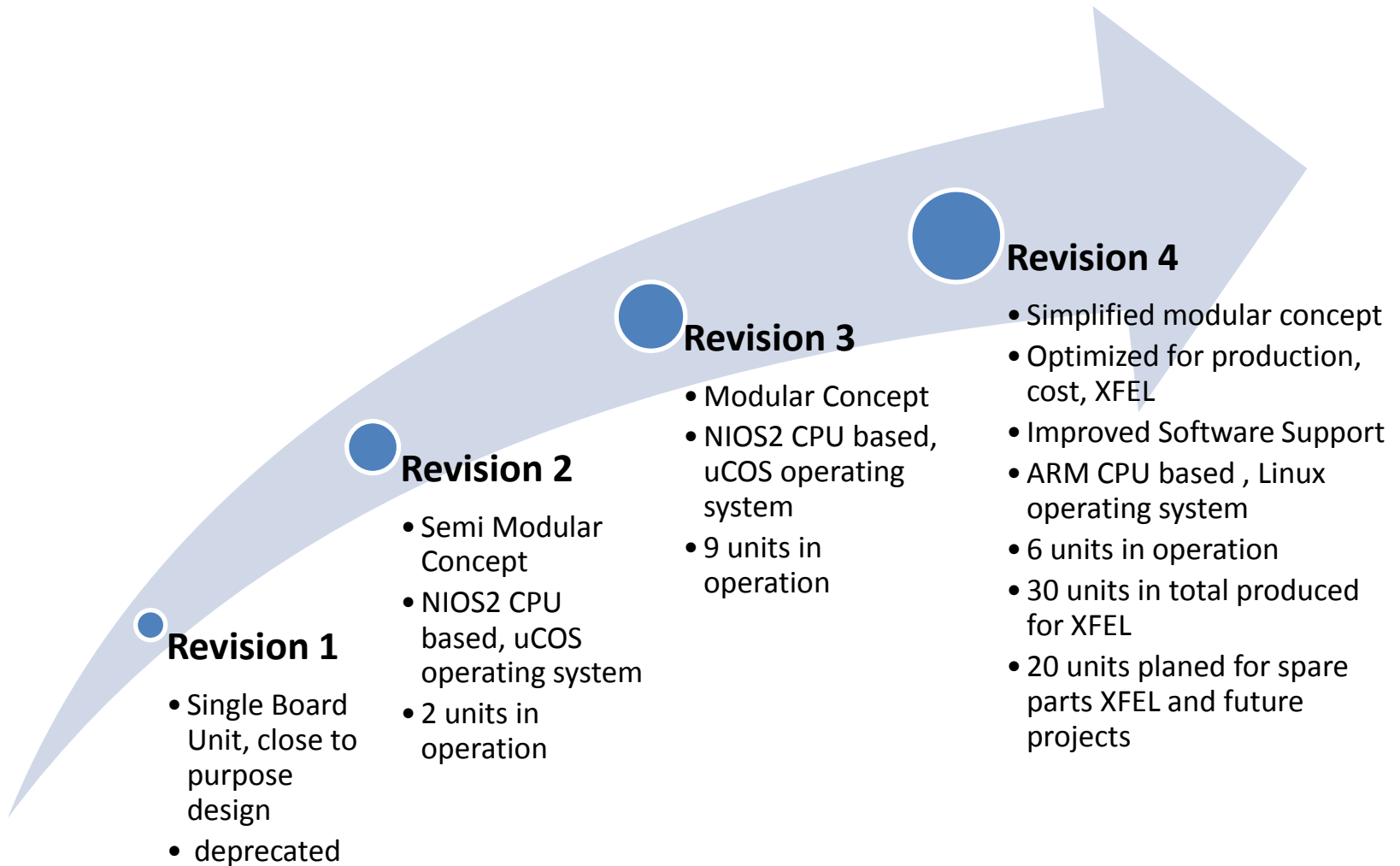
Interlock System

Interlock Function

- Protect cost intensive components in case of a technical problem
  - Klystron, Directional Coupler, Waveguide System, Cavities, etc.
- In **case of an error**, subsystems are switched off fast to prevent high energy deposition and damage
- **Main Principle**: Interlock function and logic is implemented in hardware (FPGA firmware)
- Software is used for configuration and communication

System Usage

- Designed for usage at XFEL
- Used at RF teststands
  - Klystron Teststands, XFEL accelerating module conditioning
  - PITZ (Photo Injector Teststand Zeuthen)
- Used at accelerator facilities:
  - FLASH in Hamburg
  - Since Q1 2013 – first XFEL RF System (GUN) in HH

Hardware History

Revision 1

- Single Board Unit, close to purpose design
- deprecated

Revision 2

- Semi Modular Concept
- NIOS2 CPU based, uCOS operating system
- 2 units in operation

Revision 3

- Modular Concept
- NIOS2 CPU based, uCOS operating system
- 9 units in operation

Revision 4

- Simplified modular concept
- Optimized for production, cost, XFEL
- Improved Software Support
- ARM CPU based , Linux operating system
- 6 units in operation
- 30 units in total produced for XFEL
- 20 units planed for spare parts XFEL and future projects

Interlock Crate

- 19'' 3HU crate

- 20 available slave slots

- provides many signal connections

- distribution panels connect the interlock crate with incoming and outgoing signal cables
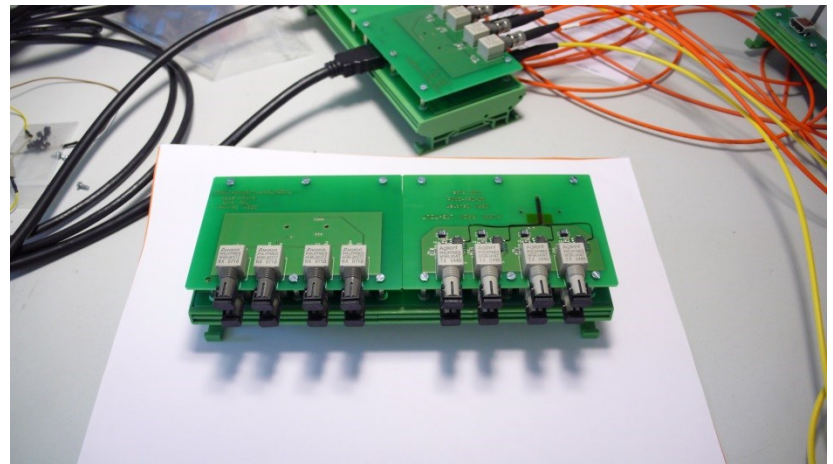 - ➢ easy access to all signal cables
  - ➢ easy module exchange

Interlock Controller
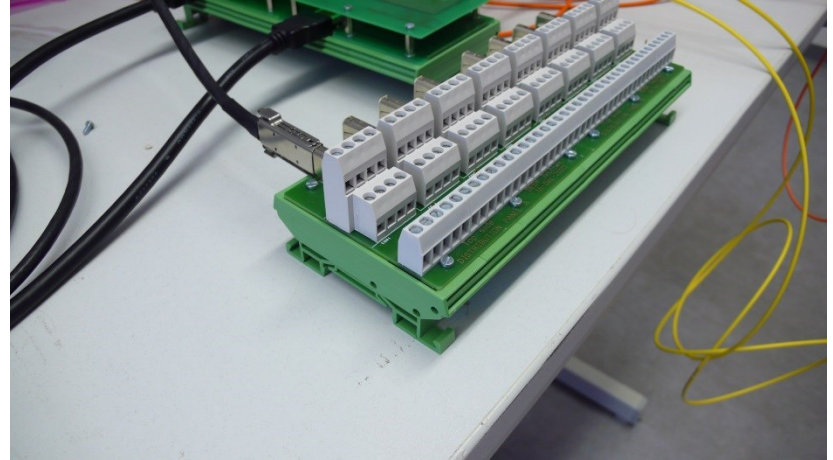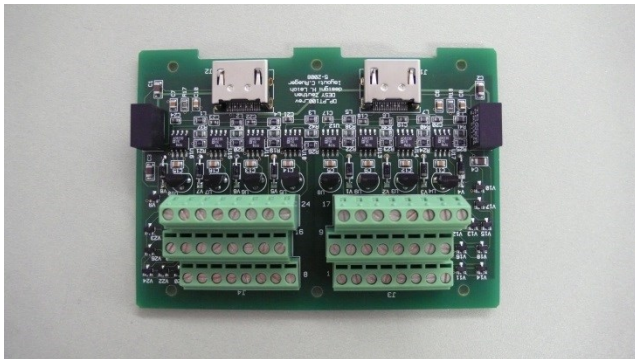
Slave Modules
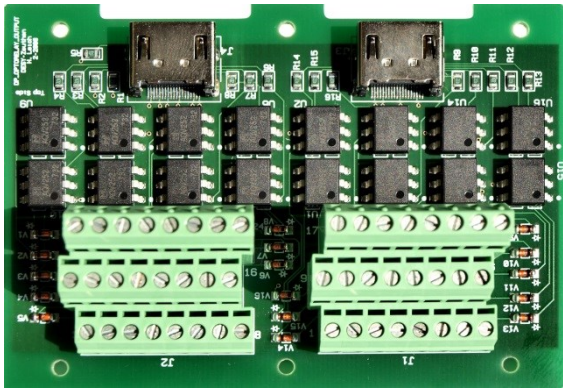
Distribution Panels
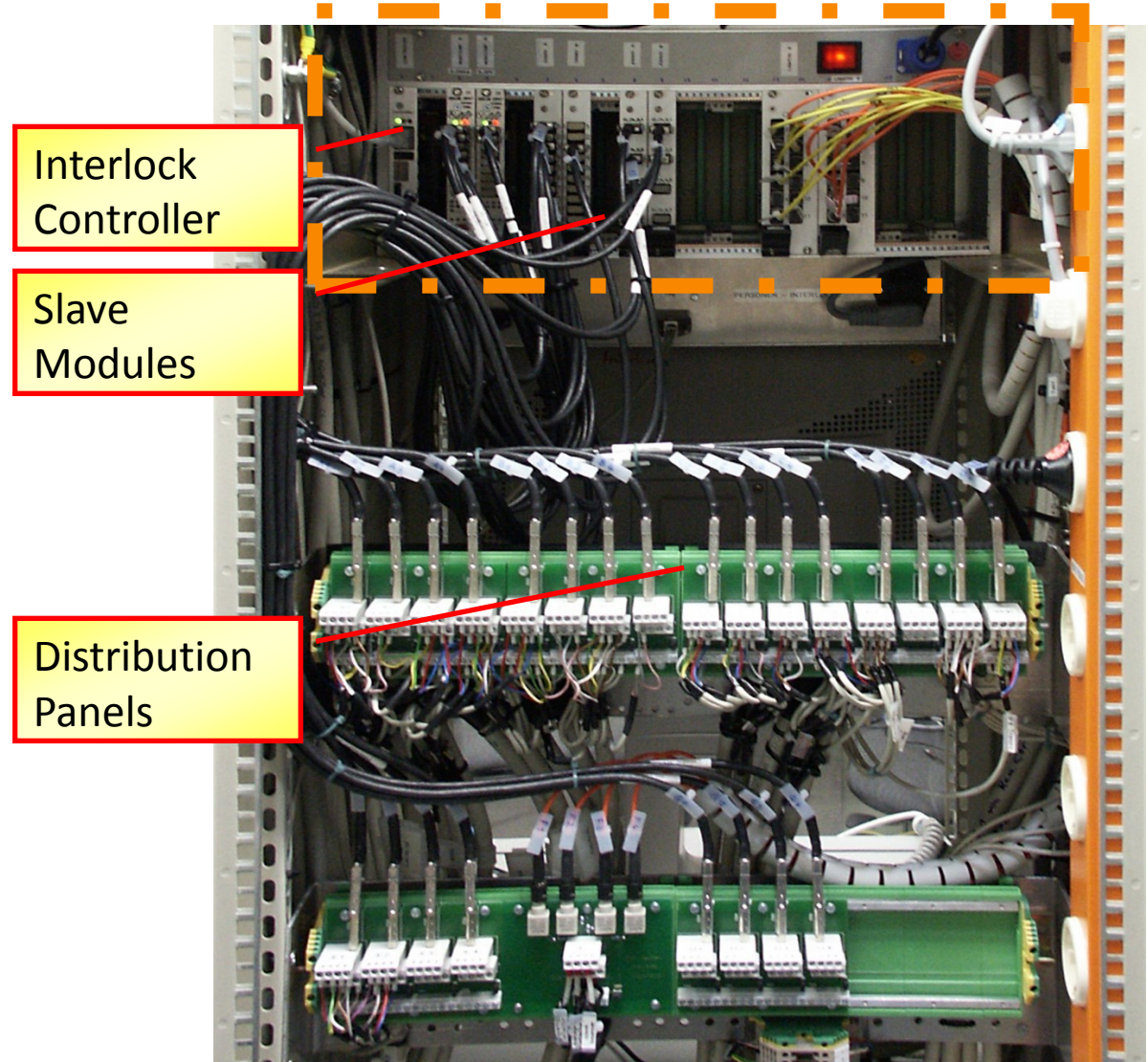
Interlock Modules

- Controller Module
  - NIOS II Processor, 64MB RAM, 16MB Flash
  - Ethernet Interface
- Slave Modules
  - Digital I/O, 32 input, 32 output channels
  - Analog window comparator, 36 input channels
  - Light I/O, 16 input, 16 output channels,
  - Analog I/O, 8 input, 8 output channels
  - Fast Analog Input, 16 channels

Interlock Rev.3 Modules

Window Comp. Typ A

Window Comp. Typ V

Digital I/O

Controller with NIOS/II

Light I/O

Analog I/O

Distribution Panels

Signal Processing

Sensors, Status of RF components

↓

Input Preprocessing

↓

Interlock Logic

↓

Generate Interlock Output Signals

↓

Enable/Disable RF Components
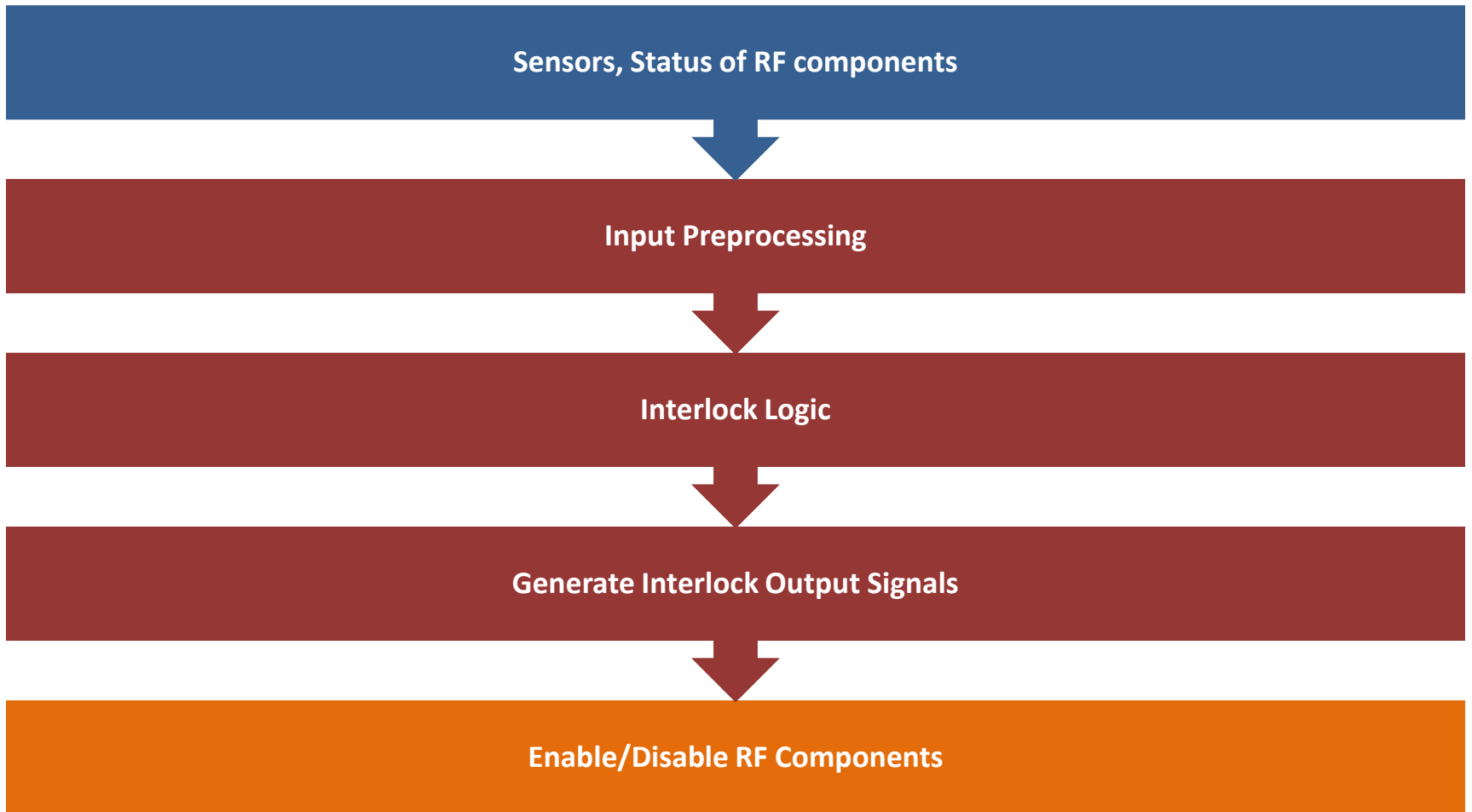
Hardware architecture overview

- interlock function completely implemented in hardware
- <u>**Strict**</u> **separation of interlock logic and processor bus**

Softcore
RISC Processor
NIOS-II

**Interlock
Controller**

Interlock Logic
in pure hardware

Backplane

cessor Bus, Interrupts and Other

Backplane

Slave I/O
Module

· · ·

Slave I/O
Module

Backplane

Backplane

Slave Expansion
Board
(optional)

Input Status Signals

Output Control Signals
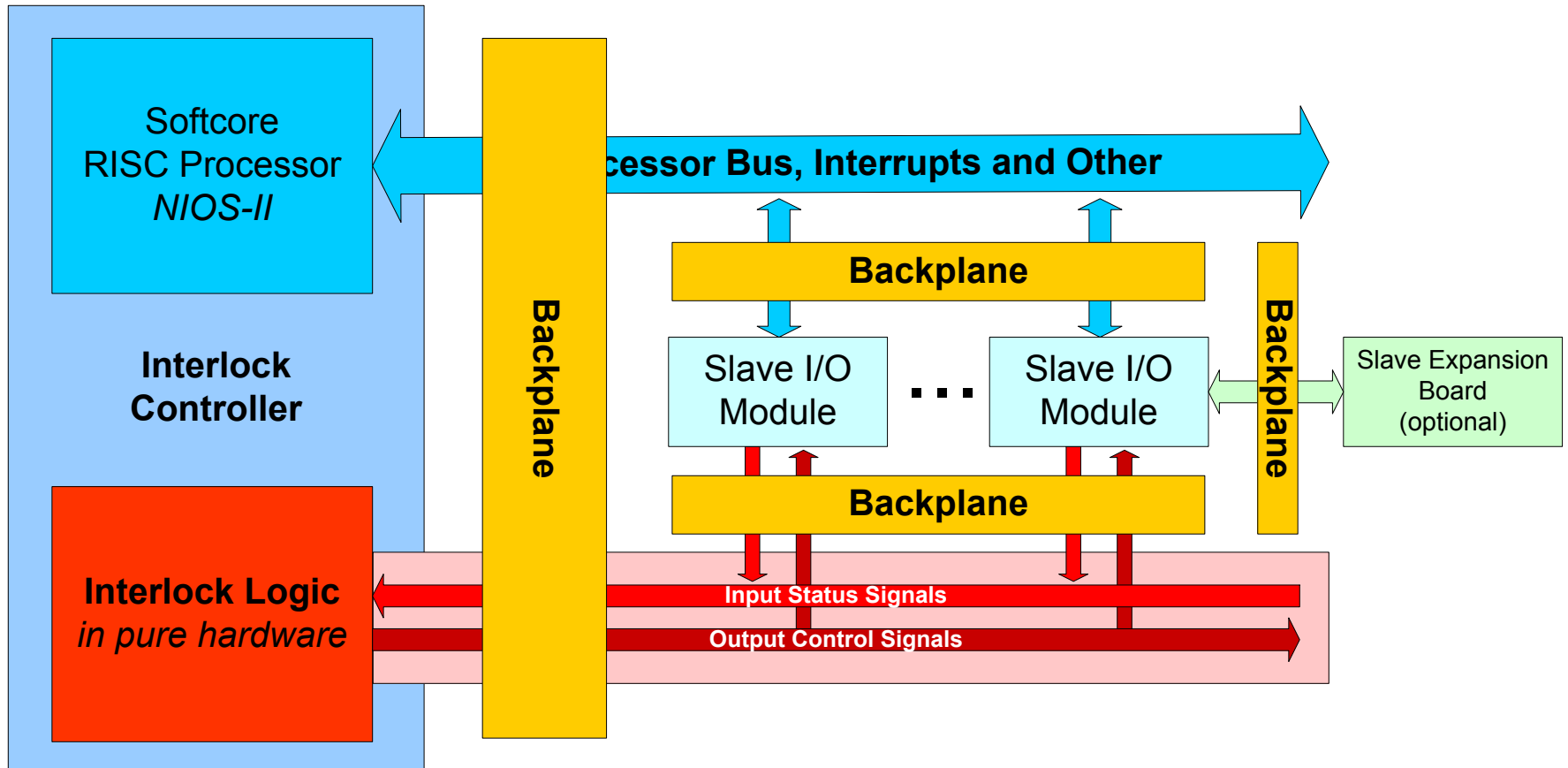
Inputs for Interlock Signals

- Water Flow sensors
- Temperature sensors
- Pressure sensors
- Radiation sensors
- RF leakage sensors
- Spark Sensors in waveguide system
- RF Powermeter measurements
- Voltage/Current measurements
- Status signals from RF components
- etc.

Features Rev. 3

- 20 Slots, 768 input signals, 768 output signals
- Catch input glitches <1us
- React within 0.25us
- Standard features
  - Configurable filter times 0ns – 1000ms for each input
  - Configurable masks for each input signal
  - Configurable thresholds
  - Limited remote firmware upgrade ability
- Customer specific extras:
  - Spark counter
  - Monoflops/Latches for specific signals
  - Custom logic to special purpose (ex.g. SF6 gas)
  - Powermeter auto-reset timer

Flexibility

- Interlock Firmware is adabtable to needs of the „customer" e.g. RF Station / Gun
- Ex.g.: Customer specific extras:
  - Spark counter
  - Monoflops/Latches for selected signals
  - Custom logic (ex.g. SF6 gas)
  - Powermeter auto-reset timer
  - **Hardware Commands (reset latches, etc.)**

Firmware PITZ RF1/RF2

- Interlock controls components:
  - Modulator
    - Disables High Voltage at Klystron and Preamplifier
    - Switched off when problem with Klystron
      - Arc in klystron and/or vaccum problem
      - Temperatures above thresholds, Waterflow problem
    - Modulator stops energy flow: stress for modulator and klystron
  - Preamplifier
    - Disables RF; but not Modulator
    - Switched off when problem with RF
      - Sparc happened in Waveguide system
      - Reflected power is to high (GUN/Cavity problem)
      - RF leakage detected

| Modulator Off | → | Action: Modulator Off |
| Preamp Off | → | Action: Preamp Off |
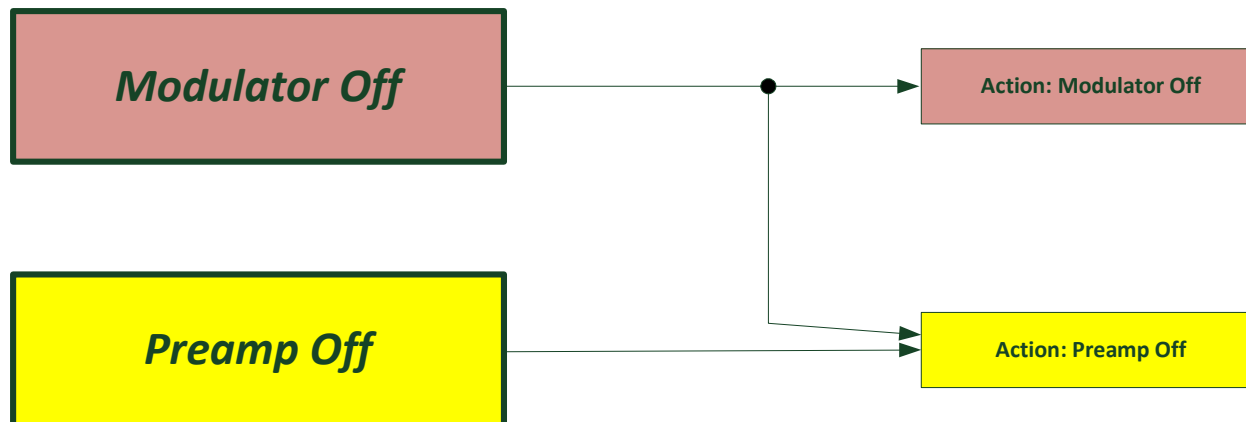
Communication

- Communication via Network Interface
- Connection to Control System DOOCS
  - Via Meta-Server
  - Update Interlock Status
  - Receive Commands

Interlock to DOOCS - Interface

- Interlock sends actual status data to Metaserver

- Metaserver integrates status-data into DOOCS-System and history

- Clients monitor signal states

DOOCS

Clients

DOOCS System

DOOCS Metaserver

HTML Browser

LabVIEW Tools

Network
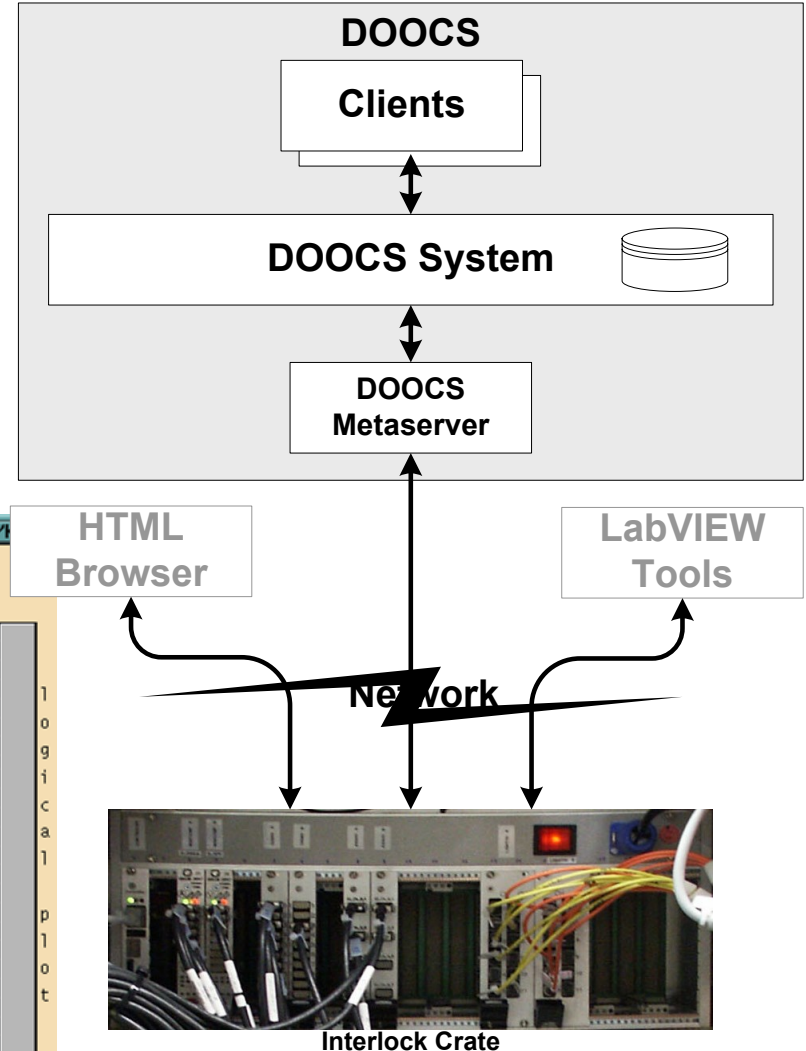
PITZ klystron interlock status   KLYS_2 / RF2 -> booster

		logical plot			logical plot
47	Current Ion Pump 3 Min		95	not used	
46	Current Ion Pump 2 Max		94	not used	
45	Current Ion Pump 2 Attention		93	not used	
44	Current Ion Pump 2 Min		92	not used	
43	Current Ion Pump 1 Max		91	Output Preamplifier Enable	
42	Current Ion Pump 1 Attention		90	Interlock Personal Signal2	
41	Current Ion Pump 1 Min		89	Interlock Personal Signal1	
40	not used		88	Clock Input Bouncer	
39	Level Klystron Tank Oil High		87	Interlock RF Leakage Detector	
38	Level Klystron Tank Oil Attention		86	Interlock Spark Detector	
37	Level Klystron Tank Oil Low		85	Status Preamplifier Ready	
36	not used		84	not used	
35	Level Transformer Tank Oil High		83	not used	
34	Level Transformer Tank Oil Attention		82	not used	
33	Level Transformer Tank Oil Low		81	not used	
32	not used		80	not used	
31	Temp Reserve 2		79	not used	
30	Temp Reserve 1		78	Power Gun Pwrmeter WG2 Reflected Max	
29	Temp Body Window 2		77	Power Gun Pwrmeter WG1 Reflected Max	
28	Temp Body Window 1		76	Power Circulator Pwrmeter WG2 Reflected Max	
27	Temp Circulator 2 Water Out		75	Power Circulator Pwrmeter WG1 Reflected Max	
26	Temp Circulator 1 Water Out		74	Power Klystron Pwrmeter WG2 Reflected Max	
25	Temp Dummy Load 2 Water Out		73	Power Klystron Pwrmeter WG1 Reflected Max	

Interlock Crate

Features Rev. 4

- Many hardware features of Interlock Rev.3
- 13 Slots, 386 input signals, 386 output signals
- checksum secured backplane communication
- 16 dedicated adc transport channels for 1MS analog data pulse recording
- SEU self detection
- Full remote firmware upgrade ability
- Trackable hardware via unique HW ID's
- linux software support (SSH, Thrift, ZMQ, etc.)